5. The apparatus of Claim 1, wherein said predictive nature of said randomization is accomplished by means for precalculating said randomization for each possible input data pattern.

6. The apparatus of Claim 5, wherein said pre-calculation is performed at a time that a new input data pattern is entered.

7. The apparatus of Claim 1, further comprising:

means for performing a full hardware calculation of expected randomization outputs for each input that is applied.

8. The apparatus of Claim 7, wherein a plurality of randomizer feedback values are evaluated in real-time when a new input is applied.

9. The apparatus of Claim 8, further comprising:

means for storing said randomizer output values in said memory for each randomizer feedback that is being considered at a time.

10. The apparatus of Claim 1, wherein said adaptive nature of said randomization is accomplished by means for adjusting said randomization, over time, to handle changing input data patterns that are to be analyzed.

11. The apparatus of Claim 1, wherein said high speed predictive nature of said system permits a significant number of possible randomization feedback paths to be maintained in said memory at any time.

12. The apparatus of Claim 1, further comprising:

means for adjusting a possible randomization feedback value after any data have been received if an existing feedback randomization is significantly less ideal than another feedback randomization that has been evaluated.

13. The apparatus of Claim 1, further comprising:

means for maintaining statistics on substantially all presently evaluated feedback randomizations to determine a best randomization, as well as any randomization that may be no longer usable.

14. The apparatus of Claim 1, further comprising:

means for quickly bringing substantially all of said input data patterns back to evaluate other possible randomization patterns when a randomization is no longer usable.

15. The apparatus of Claim 1, further comprising:

means for implementing sequential masking operations on said input data to accomplish sequential randomization of said input data patterns.

16. The apparatus of Claim 15, further comprising:

means for permitting either of fixed or programmable masking of selected bit patterns within said input data.

17. The apparatus of Claim 16, wherein said masking operations permit a user to pre-program a series of masking decisions that can result in a final input data pattern match.

18. An apparatus for rapid differentiation between input data comprised of a limited number of input data bits, comprising:

a randomizer for providing a usable feedback randomization pattern, for a random set of inputs, based upon an effective mapping of input data patterns to output vectors; and

means for handling a limited number of cases where two or more input data patterns are mapped to a same output value.

19. The apparatus of Claim 18, said means for handling further comprising:

means for permitting a set value of multiple output cases where any of two, three, or four input data patterns map to a same output pattern;

wherein said means for permitting evaluates a number of paired, tripled, and quadrupled output vectors in determining which randomizer feedback to use, as well as to determine when a randomizer feedback should be discarded.

20. The apparatus of Claim 18, said randomizer further comprising:

a primary randomizer for mapping each input data pattern to an output value;

wherein sufficient randomizer feedbacks are simultaneously evaluated to provide that a usable feedback is substantially always available.

21. The apparatus of Claim 20, said randomizer further comprising:

a secondary randomizer for differentiating between input data patterns that have been mapped to a same output value;

wherein entries in each of multiple data input patterns are different from each other.

22. The apparatus of Claim 18, wherein for a given number of output states, a given number of input data patterns, and a given number of multiple outputs, said means for handling determines a probability that any specific randomizer feedback maps said input data patterns into a usable set of output states.

23. A method for ultra-high speed data classification, comprising the steps of:

providing a data framer for framing input data;

providing a complex circuit for permitting a user to differentiate between a plurality of different patterns in said input data;

performing serial mode classification of said data to produce extremely fast characterization in a predictable timeframe by performing adaptive programmable randomization to differentiate between input vectors; and

optionally performing parallel mode classification by providing fast classification of data that have already been stored in a memory as successive parallel words of data.

24. An apparatus for ultra-high speed data classification, comprising:

a data framer;

said data framer comprising an adaptive programmable randomizer; and

a complex circuit for controlling said adaptive programmable randomizer.

25. The apparatus of Claim 24, said data framer comprising a primary and secondary randomizer that are programmably configured by said complex circuit.

26. The apparatus of Claim 25, said data framer further comprising:

a plurality of registers for setting up feedback configurations for said randomizers.

27. The apparatus of Claim 25, said data framer further comprising:

a randomizer enable control block.

28. The apparatus of Claim 27, wherein a clock to said primary and secondary randomizers is gated ON and OFF by an enable randomizer signal that is generated by said enable control block; and

wherein said enable randomizer signal is turned on at the start of a packet.

29. The apparatus of Claim 25, said data framer further comprising:

a masking control block that allows programmable, sequential, user controlled masking of groups of user defined bits.

30. The apparatus of Claim 25, said data framer further comprising:

an output register synchronization and queue that assures that said primary randomizer, said secondary randomizer, feedback registers, and masking registers are stored for each packet.

31. The apparatus of Claim 24, wherein said complex circuit maintains multiple input pattern mappings associated with different primary and secondary randomizer equations, determines a best randomizer selection, decides when to switch randomizer values, and determines when a randomizer value is no longer useful and an entirely new mapping should be generated.

32. The apparatus of Claim 24, wherein said complex circuit comprises any of the following:

a microprocessor interface for communicating to a host processor system;

a first memory interface for communicating with either of a stand alone memory or shared dual port memory, for storing data patterns to be matched;

a second memory interface for communicating with a dedicated memory that contains mappings for a plurality of primary and secondary randomizer settings; and

an interface for communicating with said data framer.

33. A method for ultra-high speed data classification, comprising the steps of:

providing a data framer for framing input data; and

providing a complex circuit for permitting a user to differentiate between a plurality of different patterns in said input data.

34. The method of Claim 33, further comprising the step of:

said user loading input patterns into said complex circuit, said patterns made up of a combination of data and, optionally, one or more masking steps that are performed on said data stream in a potentially sequential fashion, said masking steps optionally comprising mapping a range of data values to a single mask step output and, when that mask step output is reached, executing additional programmable masking or verification;

wherein said optional one or more masking steps are responsible for enabling only those input register bits that a user is interested in examining.

35. The method of Claim 34, wherein input patterns are handled by an input manager control and state machine function where they are directed into an input register.

36. The method of Claim 34, wherein said input patterns are loaded into an external memory for use in cases where a mapping is discarded and a new mapping must be generated.

37. The method of Claim 34, further comprising the step of:

providing an equation mapper for generating a related randomizer value;

wherein said equation mapper permits a randomizer value to be calculated in a single cycle by calculating randomizer mappings for different equations simultaneously;

wherein said complex circuit adjusts adaptively to select optimal randomizer settings based on input and masking patterns that have been applied to said complex circuit.

38. The method of Claim 34, further comprising the step of:

providing a mapper multiplexer for immediate selection between each of a plurality of possible randomizer outputs associated with each of a plurality of possible randomizer equations.

39. The method of Claim 36, further comprising the step of:

providing a mapper storage control and storage state machine for saving and retrieving values from a plurality of equation mapping tables.

40. The method of Claim 39, wherein said mapper storage control and storage state machine determines whether a present location pointed to by a primary randomizer value contains 0,1,2,3, or 4 entries.

41. The method of Claim 39, wherein said mapper storage control and storage state machine is responsible for handling creation and destruction of multiple entries, and adjustment of multiple entry tables that dictate those entries that are used.

42. The method of Claim 34, further comprising the step of:

providing a masking engine for permitting a user to setup sequential masking operations.

43. The method of Claim 34, further comprising the step of:

providing a time accelerator for re-mapping a received randomizer value to generate a randomizer value that would have been received if zero

values had been clocked into a randomizer for a fixed number of cycles after a received randomizer value was captured.

44. The method of Claim 34, further comprising the step of:

providing a mapper engine, statistics, and state machine for determining equations to be used, and for determining when said equations are no longer usable and need to be replaced.

45. The method of Claim 44, wherein said mapper engine, statistics, and state machine maintains statistics on all equation mappings that are maintained in a memory, selects a best mapping, and sends said to said data framer.

46. In a network for high speed transmission of digital data, said network comprising a memory, an apparatus for rapid differentiation between input data, comprising:

a module comprising functional elements for adaptive, programmable, predictive, and sequential randomization of said data; and

said module comprising at least one programmable feedback shift register that is driven by said input data, wherein a final state of said at least one shift register is used as an index into said memory to determine which if any input data pattern has been matched;

wherein input data pattern matching effects data classification.

47. The apparatus of Claim 46, wherein said at least one shift register comprises a register having at least two feedback paths that can be programmed to be enabled or disabled.

48. The apparatus of Claim 47, wherein said at least two programmable feedback paths are comprised such that output values from one feedback path are uncorrelated to output values from another feedback path.

49. The apparatus of Claim 48, wherein general probability theory to be used to evaluate randomization of said input data.

50. The apparatus of Claim 46, wherein said predictive nature of said randomization is accomplished by means for precalculating said randomization for each possible input data pattern.

51. The apparatus of Claim 50, wherein said pre-calculation is performed at a time that a new input data pattern is entered.

52. The apparatus of Claim 46, further comprising:

means for performing a full hardware calculation of expected randomization outputs for each input that is applied.

53. The apparatus of Claim 52, wherein a plurality of randomizer feedback values are evaluated in real-time when a new input is applied.

54. The apparatus of Claim 53, further comprising:

means for storing said randomizer output values in said memory for each randomizer feedback that is being considered at a time.

54. The apparatus of Claim 46, wherein said adaptive nature of said randomization is accomplished by means for adjusting said randomization, over time, to handle changing input data patterns that are to be analyzed.

55. The apparatus of Claim 46, wherein said high speed predictive nature of said system permits a significant number of possible randomization feedback paths to be maintained in said memory at any time.

56. The apparatus of Claim 46, further comprising:

means for adjusting a possible randomization feedback value after any data have been received if an existing feedback randomization is significantly less ideal than another feedback randomization that has been evaluated.

57. The apparatus of Claim 46, further comprising:

means for maintaining statistics on substantially all presently evaluated feedback randomizations to determine a best randomization, as well as any randomization that may be no longer usable.

58. The apparatus of Claim 46, further comprising:

means for quickly bringing substantially all of said input data patterns back to evaluate other possible randomization patterns when a randomization is no longer usable.

59. The apparatus of Claim 46, further comprising:

means for implementing sequential masking operations on said input data to accomplish sequential randomization of said input data patterns.

60. The apparatus of Claim 59, further comprising:

means for permitting either of fixed or programmable masking of selected bit patterns within said input data.

61. The apparatus of Claim 60, wherein said masking operations permit a user to pre-program a series of masking decisions that can result in a final input data pattern match.

62. An apparatus for rapid differentiation between input data comprised of a limited number of input data bits, comprising:

a randomizer for providing a usable feedback randomization pattern, for a random set of inputs, based upon an effective mapping of input data patterns to output vectors; and

means for handling a limited number of cases where two or more input data patterns are mapped to a same output value.

63. The apparatus of Claim 62, said means for handling further comprising:

means for permitting a set value of multiple output cases where any of two, three, or four input data patterns map to a same output pattern;

wherein said means for permitting evaluates a number of paired, tripled, and quadrupled output vectors in determining which randomizer feedback to use, as well as to determine when a randomizer feedback should be discarded.

64. The apparatus of Claim 62, said randomizer further comprising:

a primary randomizer for mapping each input data pattern to an output value;

wherein sufficient randomizer feedbacks are simultaneously evaluated to provide that a usable feedback is substantially always available.

65. The apparatus of Claim 64, said randomizer further comprising:

a secondary randomizer for differentiating between input data patterns that have been mapped to a same output value;

wherein entries in each of multiple data input patterns are different from each other.

66. The apparatus of Claim 62, wherein for a given number of output states, a given number of input data patterns, and a given number of multiple outputs, said means for handling determines a probability that any specific randomizer feedback maps said input data patterns into a usable set of output states.

67. A method for ultra-high speed data classification, comprising the steps of:

providing a data framer for framing input data;

providing a complex circuit for permitting a user to differentiate between a plurality of different patterns in said input data;

performing serial mode classification of said data to produce extremely fast characterization in a predictable timeframe by performing adaptive programmable randomization to differentiate between input vectors; and

optionally performing parallel mode classification by providing fast classification of data that have already been stored in a memory as successive parallel words of data.

68. An apparatus for ultra-high speed data classification, comprising:

a data framer;

said data framer comprising an adaptive programmable randomizer; and

a complex circuit for controlling said adaptive programmable randomizer.

69. The apparatus of Claim 68, said data framer comprising a primary and secondary randomizer that are programmably configured by said complex circuit.

70. The apparatus of Claim 69, said data framer further comprising:

a plurality of registers for setting up feedback configurations for said randomizers.

71. The apparatus of Claim 69, said data framer further comprising:

a randomizer enable control block.

72. The apparatus of Claim 71, wherein a clock to said primary and secondary randomizers is gated ON and OFF by an enable randomizer signal that is generated by said enable control block; and

wherein said enable randomizer signal is turned on at the start of a packet.

73. The apparatus of Claim 69, said data framer further comprising:

a masking control block that allows programmable, sequential, user controlled masking of groups of user defined bits.

74. The apparatus of Claim 69, said data framer further comprising:

an output register synchronization and queue that assures that said primary randomizer, said secondary randomizer, feedback registers, and masking registers are stored for each packet.

75. The apparatus of Claim 68, wherein said complex circuit maintains multiple input pattern mappings associated with different primary and secondary randomizer equations, determines a best randomizer selection, decides when to switch randomizer values, and determines when a randomizer value is no longer useful and an entirely new mapping should be generated.

76. The apparatus of Claim 68, wherein said complex circuit comprises any of the following:

a microprocessor interface for communicating to a host processor system;

a first memory interface for communicating with either of a stand alone memory or shared dual port memory, for storing data patterns to be matched;

a second memory interface for communicating with a dedicated memory that contains mappings for a plurality of primary and secondary randomizer settings; and

an interface for communicating with said data framer.

77. A method for ultra-high speed data classification, comprising the steps of:

providing a data framer for framing input data; and

providing a complex circuit for permitting a user to differentiate between a plurality of different patterns in said input data.

78. The method of Claim77, further comprising the step of:

said user loading input patterns into said complex circuit, said patterns made up of a combination of data and, optionally, one or more masking steps that are performed on said data stream in a potentially sequential fashion, said masking steps optionally comprising mapping a range of data values to a single mask step output and, when that mask step output is reached, executing additional programmable masking or verification;

wherein said optional one or more masking steps are responsible for enabling only those input register bits that a user is interested in examining.

79. The method of Claim 78, wherein input patterns are handled by an input manager control and state machine function where they are directed into an input register.

80. The method of Claim 78, wherein said input patterns are loaded into an external memory for use in cases where a mapping is discarded and a new mapping must be generated.

81. The method of Claim 78, further comprising the step of:

providing an equation mapper for generating a related randomizer value;

wherein said equation mapper permits a randomizer value to be calculated in a single cycle by calculating randomizer mappings for different equations simultaneously;

wherein said complex circuit adjusts adaptively to select optimal randomizer settings based on input and masking patterns that have been applied to said complex circuit.

82. The method of Claim 78, further comprising the step of:

providing a mapper multiplexer for immediate selection between each of a plurality of possible randomizer outputs associated with each of a plurality of possible randomizer equations.

83. The method of Claim 82, further comprising the step of:

providing a mapper storage control and storage state machine for saving and retrieving values from a plurality of equation mapping tables.

84. The method of Claim 83, wherein said mapper storage control and storage state machine determines whether a present location pointed to by a primary randomizer value contains 0,1,2,3, or 4 entries.

85. The method of Claim 83, wherein said mapper storage control and storage state machine is responsible for handling creation and destruction of multiple entries, and adjustment of multiple entry tables that dictate those entries that are used.

86. The method of Claim 78, further comprising the step of:

providing a masking engine for permitting a user to setup sequential masking operations.

87. The method of Claim 78, further comprising the step of:

providing a time accelerator for re-mapping a received randomizer value to generate a randomizer value that would have been received if zero values had been clocked into a randomizer for a fixed number of cycles after a received randomizer value was captured.

88. The method of Claim 78, further comprising the step of:

providing a mapper engine, statistics, and state machine for determining equations to be used, and for determining when said equations are no longer usable and need to be replaced.

89. The method of Claim 82, wherein said mapper engine, statistics, and state machine maintains statistics on all equation mappings that are maintained in a memory, selects a best mapping, and sends said to said data framer.